

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4094 8-stage shift-and-store bus register

Product specification
File under Integrated Circuits, IC06

December 1990

8-stage shift-and-store bus register

74HC/HCT4094

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the "4094" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP_0 to QP_7). The parallel outputs may be connected directly to common bus lines. Data is shifted on the positive-going clock (CP) transitions.

QUICK REFERENCE DATA

$GND = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to QS_1	$C_L = 15 \text{ pF}$; $V_{CC} = 5 \text{ V}$	15	19	ns
	CP to QS_2		13	18	
	CP to QP_n		20	21	
	STR to QP_n		18	19	
	maximum clock frequency		95	86	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	83	92	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP ₀ to QP ₇	parallel outputs
8	GND	ground (0 V)
9, 10	QS ₁ , QS ₂	serial outputs
15	OE	output enable input
16	V _{CC}	positive supply voltage

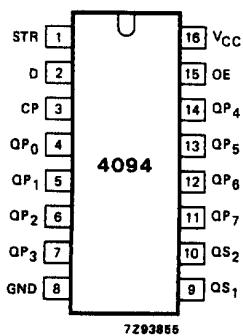


Fig.1 Pin configuration.

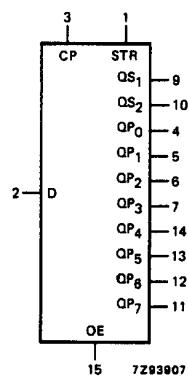


Fig.2 Logic symbol.

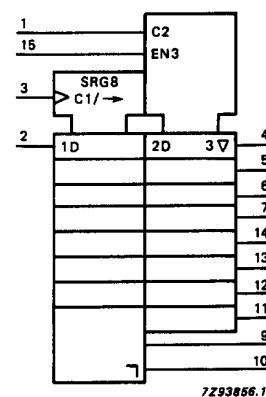


Fig.3 IEC logic symbol.

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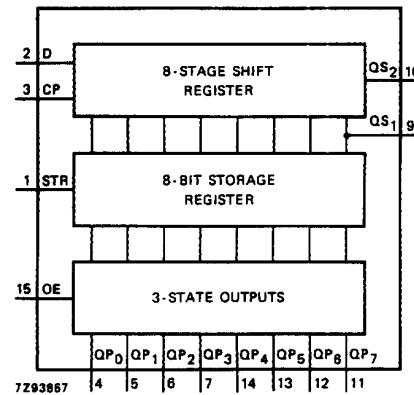


Fig.4 Functional diagram.

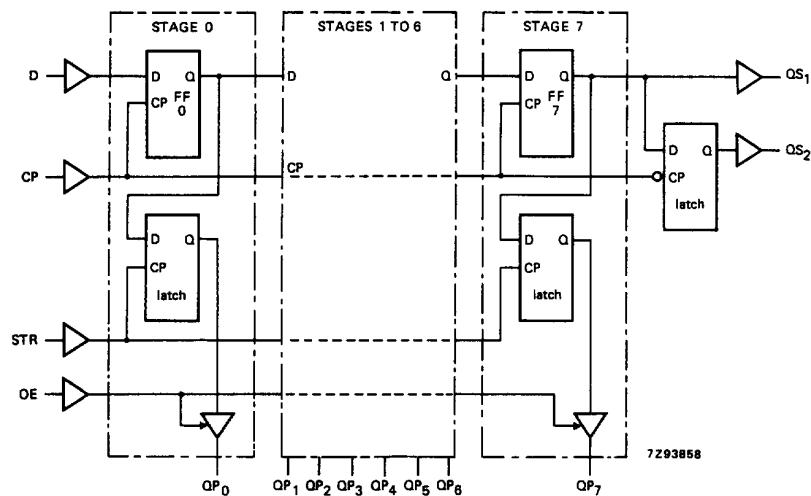


Fig.5 Logic diagram.

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FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP ₀	QP _n	QS ₁	QS ₂
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	QP ₇
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	QP _{n-1}	Q'6	NC
↑	H	H	H	H	QP _{n-1}	Q'6	NC
↓	H	H	H	NC	NC	NC	QP ₇

Notes

1. H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

NC = no change

↑ = LOW-to-HIGH CP transition

↓ = HIGH-to-LOW CP transition

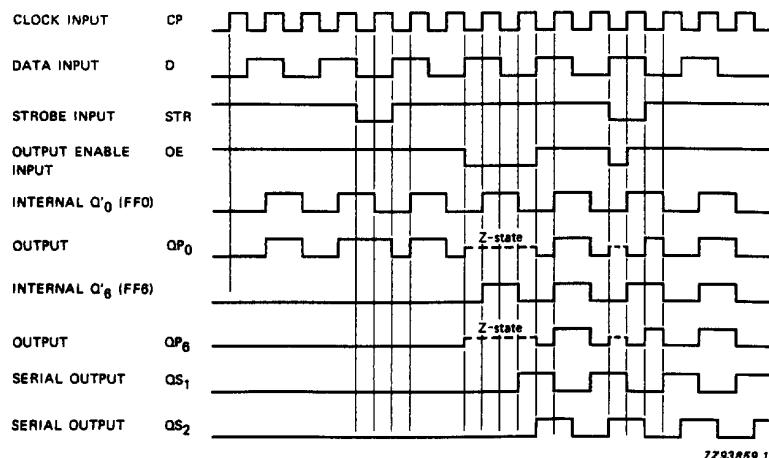
Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QS_n output at the positive clock edge

Fig.6 Timing diagram.

8-stage shift-and-store bus register

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay CP to QS ₁		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0		
t _{PHL} / t _{PLH}	propagation delay CP to QS ₂		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0		
t _{PHL} / t _{PLH}	propagation delay CP to QP _n		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0		
t _{PHL} / t _{PLH}	propagation delay STR to QP _n		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0		
t _{PZH} / t _{PZL}	3-state output enable time OE to QP _n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0		
t _{PHZ} / t _{PLZ}	3-state output disable time OE to QP _n		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0		
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5		
t _W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0		
t _W	strobe pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0		
t _{su}	set-up time D to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0		
t _{su}	set-up time CP to STR	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0		

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SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _h	hold time D to CP	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0		
t _h	hold time CP to STR	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0		
f _{max}	maximum clock pulse frequency	6.0 30 35	28 87 103		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0		

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DC CHARACTERISTICS FOR 74HCTFor the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I_{CC} category: MSI**Note to HCT types**The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE, CP	1.50
D	0.40
STR	1.00

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay CP to QS_1	23	39		49		59	ns	4.5	Fig.7		
t_{PHL}/ t_{PLH}	propagation delay CP to QS_2	21	36		45		54	ns	4.5	Fig.7		
t_{PHL}/ t_{PLH}	propagation delay CP to QP_n	25	43		54		65	ns	4.5	Fig.7		
t_{PHL}/ t_{PLH}	propagation delay STR to QP_n	22	39		49		59	ns	4.5	Fig.8		
t_{PZH}/ t_{PZL}	3-state output enable time OE to QP_n	20	35		44		53	ns	4.5	Fig.9		
t_{PHZ}/ t_{PLZ}	3-state output disable time OE to QP_n	21	35		44		53	ns	4.5	Fig.9		
t_{THL}/ t_{TLH}	output transition time	7	15		19		22	ns	4.5	Fig.7		
t_W	clock pulse width HIGH or LOW	16	7		20		24	ns	4.5	Fig.7		
t_W	strobe pulse width HIGH	16	5		20		24	ns	4.5	Fig.8		
t_{su}	set-up time D to CP	10	4		13		15	ns	4.5	Fig.10		
t_{su}	set-up time CP to STR	20	9		25		30	ns	4.5	Fig.8		
t_h	hold time D to CP	4	0		4		4	ns	4.5	Fig.10		
t_h	hold time CP to STR	0	-4		0		0	ns	4.5	Fig.8		
f_{max}	maximum clock pulse frequency	30	80		24		20	MHz	4.5	Fig.7		

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AC WAVEFORMS

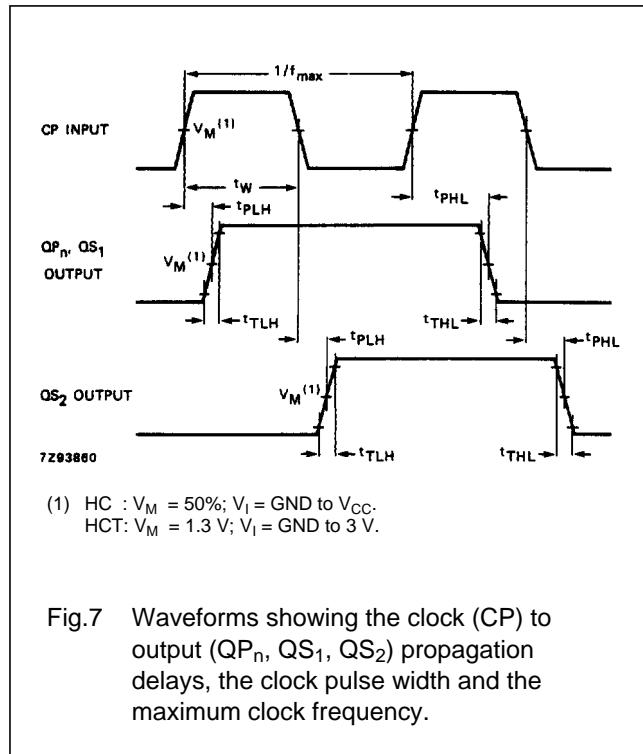


Fig.7 Waveforms showing the clock (CP) to output (QP_n , QS_1 , QS_2) propagation delays, the clock pulse width and the maximum clock frequency.

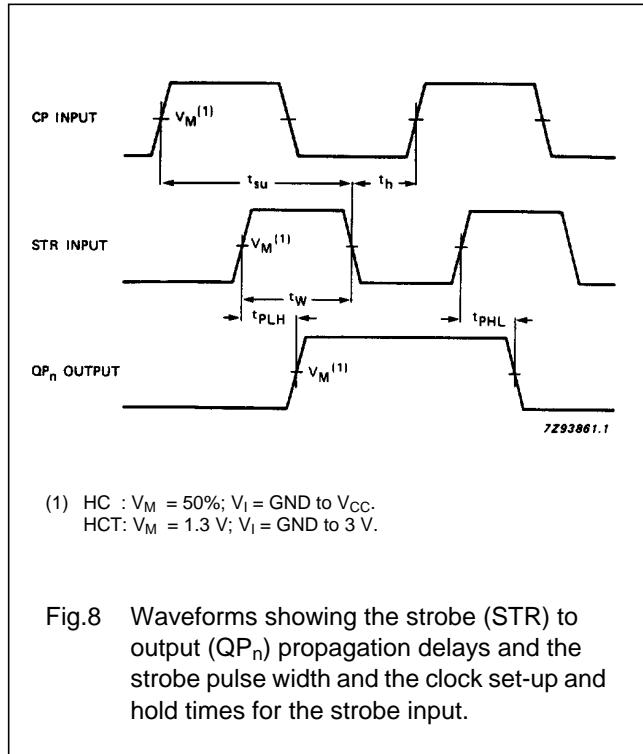


Fig.8 Waveforms showing the strobe (STR) to output (QP_n) propagation delays and the strobe pulse width and the clock set-up and hold times for the strobe input.

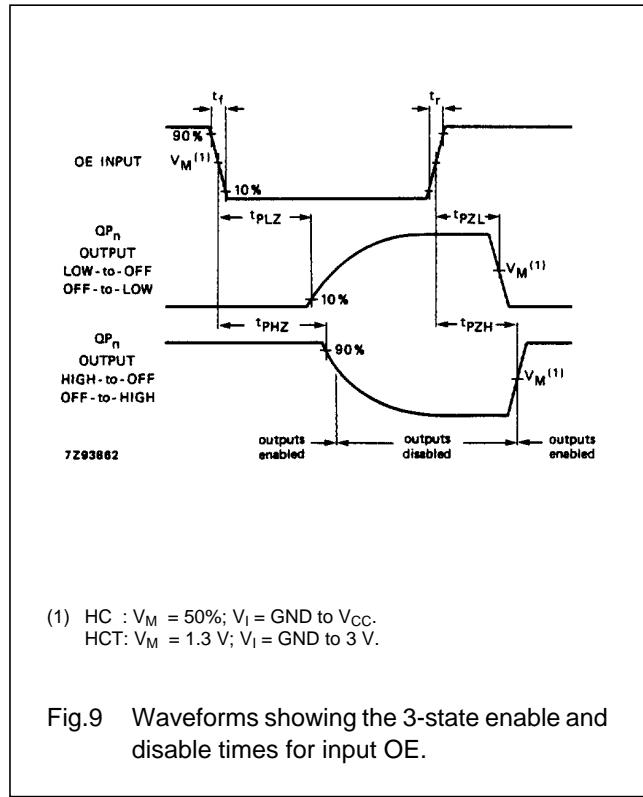


Fig.9 Waveforms showing the 3-state enable and disable times for input OE.

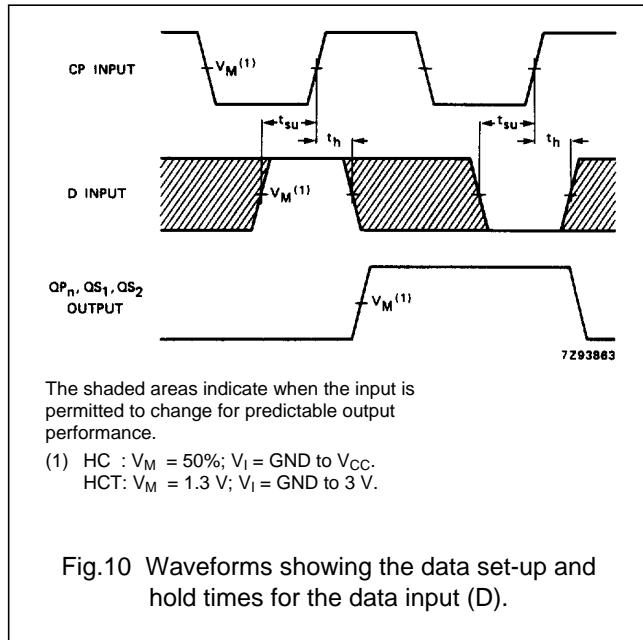


Fig.10 Waveforms showing the data set-up and hold times for the data input (D).

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".